**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: Zbiciak | Art Unit: 2124 |
| Serial No.: 09/703,034 | Examiner: Chat C. Do |
| Filed: October 31, 2000 | Docket: TI-30553 |

For: MICROPROCESSOR WITH ROUNDING DOT PRODUCT INSTRUCTION

**Reply Brief under 37 C.F.R. §41.41(a)(1)**

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Applicant's Reply Brief filed pursuant to 37 C.F.R. §41.41(a)(1) in response to new grounds of rejection and new points of argument set forth in the EXAMINER'S ANSWER of June 12, 2008.

Response to New Point of Argument

The EXAMINER'S ANSWER states at page 16, lines 7 to 21:

> "The applicant argues in pages 16-18 for claim 13 rejected under 35 U.S.C. 103(a) that the primary reference by Saishi et al. fails to disclose the adder/subtractor circuit includes a 'mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction'.
>
> "The Examiner respectfully submits that the current language does not clearly address when (e.g. before the multiplication, during the multiplication, or after the multiplication) the predetermined bit is determined for adding or inserting a carry input bit. Thus as long as a carry bit is appropriately added to min-position of result, it meets the limitations cited in the claim. Further the position to add the carry bit in the primary reference is not randomly determined but rather it is either algorithm/desired determined/calculated right before the adding process. The paragraph in column 8 lines 27-40 with support of Figure 8 clearly indicated a mid-position rounding wherein the predetermined rounding position 811 (e.g. lines 29-30 in column 8) is located at the mth bit wherein the kth bit can be set at 0. Generally by having or setting the (m+k)-th bit as m-th bit (e.g. k=0) in Figure 8m then the rounding will occur at the mid-position.

The EXAMINER'S ANSWER includes similar language regarding claim 25 at page 19, line 17 to page 20, line 11. The statements regarding when the shift is predetermined represents a new argument never before presented by the Examiner. The Applicant's arguments cited in these portions of the EXAMINER'S ANSWER were previously presented in at: page 5, line 13 to page 6, line 24 of the response filed June 6, 2006; page 4, line 14 to page 6, line 14 of the response filed October 10, 2006; page 6, line 7 to page 8, line 9 of the response filed November 8, 2006; page 7, line 27 to page 9, line 24 of the response filed April 9, 2007; and page 12, line 5 to page 14, line 13 of the response filed October 8, 2007. Accordingly, the Examiner had ample prior opportunity to present this argument but did not.

The Applicant submits that the Examiner has misconstrued this argument. The Applicant has not stated that the timing of the determination of "the predetermined bit" is important or that claims 13 and 25 differ from the reference Saishi et al. The citation of the teaching of shifting in Saishi et al is directed to another purpose. The Applicants submit that this teaching of Saishi et al makes clear that rounding signal 806 is a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Note that the teaching of Saishi et al at column 8, lines 33 and 34:

> "a signal having "1" at the (m+k) th bit is generated as the rounding signal"

supports the Applicant's understanding of the rounding signal. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an addition means. Saishi et al never states that the rounding signal is input to "a mid-position carry input to a predetermined bit" as recited in claims 13 and 25.

In view of the foregoing arguments, the Applicant respectfully submits that claims are allowable for the reasons set forth above. Accordingly, the Applicant respectfully requests reversal of the final rejection and advance to issue.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

/Robert D. Marshall, Jr./
Robert D. Marshall, Jr.
Reg. No. 28,527